Annexure 35.2

# Avinashilingam Institute for Home Science and Higher Education for Women

(Deemed to be University under Category 'A' by MHRD, Estd. u/s 3 of UGC Act 1956,
Re-accredited with 'A+' Grade by NAAC, Recognised by UGC u/s 12B)
Coimbatore - 641 043, Tamil Nadu, India.

**School of Engineering**
**M.E. VLSI Design**

**Programme Specific Outcomes:**

**PSO1:** Graduates will be able to design VLSI circuits to optimize power and area requirements, free from faults and dependencies by modeling simulation and testing.

**PSO2:** Graduates will be able to apply advanced concepts of VLSI in providing optimized solutions to industrial and socio-commercial problems.

**Scheme of Instruction & Examination**
(For students admitted from 2019-20 and onwards)

| *Part* | *Course Code* | *Name of Course /Component* | *Hours of Instruction/week* | | *Scheme of Examination* | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | *T* | *P* | *Duration of exam* | *CIA* | | *CE* | | *Total* | *Credit* |
| | | | | | | T | P | T | P | | |
| **First Semester** | | | | | | | | | | | |
| **I** | **Core Courses (CC)** | | | | | | | | | | |
| | 19MEVC01 | Graph Theory and Optimization Techniques | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | 19MEVC02 | VLSI Subsystem Design | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | 19MEVC03 | VLSI Design Practicals- I | - | 3 | 3 | - | 40 | - | 60 | 100 | 1.5 |
| | 19MEVC04 | Microcontrollers and Programmable Digital Signal Processors Practicals | - | 3 | 3 | - | 40 | - | 60 | 100 | 1.5 |
| | 19MEVC05 | Research Methodology and IPR | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | **Program Electives (PE)** | | | | | | | | | | |
| | 19MEVE11/ 19MEVE12/ 19MEVE13 | Program Elective-I | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | 19MEVE21/ 19MEVE22/ 19MEVE23 | Program Elective-II | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| **II** | **Non Credit Mandatory Courses (NCMC)** | | | | | | | | | | |
| | **Audit Course (AC)** | | | | | | | | | | |
| | 19MEMA11 / 19MEMA12 | Audit Course-I | 3 | - | 2 | 100 | - | - | - | 100 | Remark |
| | **Extracurricular Course (ECC)** | | | | | | | | | | |
| | 19MECS01 | CSS | 2 | | - | | | | | | - |

**Program Elective I**: 19MEVE11 Computer Aided Design of VLSI Systems / 19MEVE12 Hardware Description Languages / 19MEVE13 VLSI Signal Processing

**Program Elective II**: 19MEVE21 Microcontrollers and Programmable Digital Signal Processors / 19MEVE22 Digital System Design/ 19MEVE23 Neural Networks for VLSI

| *Part* | *Course Code* | *Name of Course /Component* | *Hours of Instruction/week* | | *Scheme of Examination* | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **T** | **P** | *Duration of exam* | *CIA* | | *CE* | | *Total* | *Credit* |
| | | | | | | **T** | **P** | **T** | **P** | | |
| **Second Semester** | | | | | | | | | | | |
| **I** | **Core Courses (CC)** | | | | | | | | | | |
| | 19MEVC06 | Analog VLSI Circuits | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | 19MEVC07 | Testing and Testability | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | 19MEVC08 | VLSI Design Practicals - II | - | 3 | 3 | - | 40 | - | 60 | 100 | 1.5 |
| | 19MEVC09 | VLSI Design Verification and Testing Practicals | - | 3 | 3 | - | 40 | - | 60 | 100 | 1.5 |
| | 19MEVC10 | Mini Project with Seminar | - | 2 | - | - | 100 | - | - | 100 | 1 |
| | **Professional Certification Course(PCC)** | | | | | | | | | | |
| | 19MEVP01 | Professional Certification Course | - | - | - | 100 | - | - | - | 100 | 2 |
| | **Program Electives (PE)** | | | | | | | | | | |
| | 19MEVE31/ 19MEVE32/ 19MEVE33 | Program Elective-III | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | 19MEVE41/ 19MEVE42/ 19MEVE43 | Program Elective-IV | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| **II** | **Non Credit Mandatory Courses (NCMC)** | | | | | | | | | | |
| | **Audit Course(AC)** | | | | | | | | | | |
| | 19MEMA21/ 19MEMA22 | Audit Course-II | 3 | - | 2 | 100 | - | - | - | 100 | Remark |
| | **Extracurricular Course (ECC)** | | | | | | | | | | |
| | 19MECS01 | CSS | 2 | - | 2 | 50 | 50 | - | - | 100 | Remark |
| **Internship during summer vacation for one month** | | | | | | | | | | | |

**Program Elective III**: 19MEVE31 Image Security / 19MEVE32 Design concepts in VLSI / 19MEVE33 Mixed Signal VLSI Design

**Program Elective IV**: 19MEVE41 Low Power VLSI Design / 19MEVE42 ASIC Design / 19MEVE43 High Speed VLSI

| **Third Semester** | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **I** | **Core Courses (CC)** | | | | | | | | | | |
| | 19MEVC11 | Dissertation - I | - | 20 | - | - | 100 | - | - | 100 | 10 |
| | 19MEVC12 | Internship | - | - | - | - | 100 | - | - | 100 | 1 |
| | **Program Electives (PE)** | | | | | | | | | | |
| | 19MEVE51/ 19MEVE52/ 19MEVE53 | Program Elective-V | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |
| | **Open Electives (OE)** | | | | | | | | | | |
| | 19MEBO01/ 19MEOO01/ 19MEFO01 | Open Elective | 4 | - | 3 | 40 | - | 60 | - | 100 | 4 |

**Program Elective V**: 19MEVE51 VLSI Digital Signal Processing systems / 19MEVE52 Genetic Algorithms and their Applications in VLSI / 19MEVE53 Computational Aspects of VLSI

**Open Elective**: 19MEBO01 Quality Assurance and Safety in Hospitals / 19MEOO01 Web Mining / 19MEFO01 Industrial Safety and GMP in Food Industries

| *Part* | *Course Code* | *Name of Course /Component* | *Hours of Instruction/week* | | *Scheme of Examination* | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **T** | **P** | *Duration of exam* | *CIA* | | *CE* | | *Total* | *Credit* |
| | | | | | | **T** | **P** | **T** | **P** | | |
| **Fourth Semester** | | | | | | | | | | | |
| I | **Core Course (CC)** | | | | | | | | | | |
| | 19MEVC13 | Dissertation - II | - | 32 | - | - | 200 | - | 200 | 400 | 16 |
| | | | | | | | | | | **Total** | **80** |

**Total credits required to earn the degree: 80 and successful completion of Non-Credit Mandatory Courses**

**Other course to be undergone by the students: MOOC Course – 2 credits**

**List of Program Electives (PE)**

| S. No. | *Course Code* | *Name of Course* |
|---|---|---|
| 1. | 19MEVE11 | Computer Aided Design of VLSI Systems |
| 2. | 19MEVE12 | Hardware Description Languages |
| 3. | 19MEVE13 | VLSI Signal Processing |
| 4. | 19MEVE21 | Microcontrollers and Programmable Digital Signal Processors |
| 5. | 19MEVE22 | Digital System Design |
| 6. | 19MEVE23 | Neural Networks for VLSI |
| 7. | 19MEVE31 | Image Security |
| 8. | 19MEVE32 | Design concepts in VLSI |
| 9. | 19MEVE33 | Mixed Signal VLSI Design |
| 10. | 19MEVE41 | Low Power VLSI Design |
| 11. | 19MEVE42 | ASIC Design |
| 12. | 19MEVE43 | High Speed VLSI |
| 13. | 19MEVE51 | VLSI Digital Signal Processing systems |
| 14. | 19MEVE52 | Genetic Algorithms and their Applications in VLSI |
| 15. | 19MEVE53 | Computational Aspects of VLSI |

**Open Elective (OE)**

| S. No. | Course Code | Course Title |
|---|---|---|
| 1. | 19MELO01 | Waste to Energy |

**List of Audit Courses (Non-Credit Mandatory Course)**

| S. No. | Course Code | Audit Course-I |
|---|---|---|
| 1. | 19MEMA11 | English for Research Paper Writing |
| 2. | 19MEMA12 | Disaster Management |

| S. No. | Course Code | Audit Course-II |
|---|---|---|
| 1. | 19MEMA21 | Pedagogy Studies |
| 2. | 19MEMA22 | Value Education |

***Any one Course by MOOC from SWAYAM (NPTEL)**

| S. No. | Course Code | Course Title |
|---|---|---|
| 1. | 19MEVMC1 | MOOC* (Title of the Course completed with certificate) |

## Graph Theory and Optimization Techniques

**Semester I** **Hours of Instruction / week: 4T**
**19MEVC01** **No. of Credits: 4**

**Objective:**

To study the design of VLSI circuits using Various Classification of Graphs with its Algorithm.

**Unit I Basic Concepts in Graph Theory 12**

Undirected graph – degree of a vertex, degree sequence, sub graphs, vertex induced sub graphs, complement of a graph, self complementary graphs, walk, path, connectivity, eccentricity, radius, diameter, vertex and edge cuts, vertex partition, independent set, clique. Digraph – orientation, strongly, weakly and unilaterally connected digraphs, directed acyclic graph (self study). Adjacency matrix and incidence matrix of graphs. Trees, spanning trees, matrix tree theorem.

**Unit II Special Classes of Graphs 12**

Complete graphs, bipartite graphs, grid graphs, Eulerian graphs - Euler's theorem. Hamiltonian graphs – Dirac's and Ore's theorems, closure of a graph, Bondy-Chvatal theorem, traveling salesman problem. Planar graphs – Euler's formula, Kuratowski's theorem, embedding, dual, five color and four color theorems (without proof). Overlap graph, containment graph (self study), interval graph, permutation graph, neighborhood graph and rectangular dual, relationship between these graph classes.

**Unit III Graph Algorithms in VLSI Physical Design 12**

Search algorithms – depth first search and breadth first search(self study), spanning tree algorithms – Kruskal and Prim, shortest path algorithms – Dijkstra and Floyd-Warshall, vertex coloring – Welsh-Powell algorithm, matching, perfect matching, bipartite matching – augmenting path algorithm, min-cut and max_cut algorithms.

**Unit IV Linear Programming 12**

Definition, simplex, two-phase simplex and dual simplex algorithms (self study).

**Unit V Dynamic Programming 12**

Multistage decision process, computational procedure, final and initial value problems, continuous dynamic programming, discrete dynamic programming (self study).

**Total Hours: 60**

**References:**


1. **Sherwani N A,** ***"Algorithms for VLSI Physical Design Automation",*** Springer-Verlag, 2007.
2. **Taha H A,** ***"Operations Research",*** Prentice Hall, 2003.
3. **West D B,** ***"Introduction to Graph Theory",*** Pearson Education, 2007.
4. **Yellen J and Gross J,** ***"Graph Theory and its Applications",*** Chapman & Hall, 2006.
5. **Gerez S H,** ***"Algorithms for VLSI Design Automation",*** John Wiley, 2007.
6. **Kocay W and Kreher D L,** ***"Graphs, Algorithms and Optimization",*** Chapman & Hall, 2005.
7. **Papadimitriou C H and Steiglitz K,** ***"Combinatorial Optimization",*** Prentice Hall, 1997.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand the basic concepts in Graph Theory.
CO2: Expose to special classes of graphs.
CO3: Apply graph algorithms in VLSI physical Design.
CO4: Formulate and solve linear programming Problems using various optimization techniques.
CO5: Solve and apply Dynamic Programming Problems in decision making problems.

## VLSI Subsystem Design

**Semester I** **Hours of Instruction / week: 4T**
**19MEVC02** **No. of Credits: 4**

**Objective:**

To learn the VLSI design process, design rules, characteristic of nMOS and CMOS Inverter and to design combinational logic, sequential logic and subsystems in VLSI.

**Unit I Overview of VLSI Design Methodology 12**

VLSI design process - Architectural design - Logical design - Physical design - Layout styles.Full custom, Semicustom approaches.

**LAYOUT DESIGN RULES:** Need for design rules - Mead Conway design rules for silicon gate nMOS process - CMOS n well / p well design rules(self study) - Simple layout examples - Sheet resistance - Area capacitance - Wiring capacitance- Driving large capacitive loads.

**Unit II MOS Inverter 12**

MOS device equations-nMOS inverter - steered input to an nMOS inverter - Depletion mode pull up - Enhancement mode pull ups(self study) - CMOS inverter - DC characteristics-inverter delay.

**Unit III Logic Design 12**

Pass transistor and transmission gate – Gate logic-NAND gate-NOR gate - static CMOS design, Pseudo nMOS, dynamic CMOS logic - Clocked CMOS logic - Precharged domino logic(self study) – Simple combinational logic design examples – Parity generator - Multiplexers.

**Unit IV Sequential Logic 12**

Clocked sequential circuits - Two phase clocking - charge storage – Dynamic register element – nMOS and CMOS Dynamic shift register – D and JK Flip-flop circuit - Memory Design – RAM design-CAM design(self study).

**Unit V VLSI Building Blocks Design 12**

Adders, Shifters, PLA design - Arithmetic logic Unit design – Multipliers - Serial parallel multiplier – Pipelined array multiplier (self study) - Modified Booth's Algorithm.

**Total Hours:60**

**References:**


1. **Jan M Rabaey,** ***"Digital Integrated circuits - A design",*** Prentice Hall, Dec 2004.
2. **Kang,** ***"CMOS Digital integrated Circuits",*** McGraw Hill, 2002.
3. **Neil Weste and Kamran Eshranghian** ***"Principles of CMOS VLSI Design",*** Addison Wesley, 2000.
4. **Saida M Sait and Habib Youssef,** ***"VLSI Physical Design Automation: Theory and Practice",*** World Scientific Publishing Company, 1st edition Nov 1999.
5. **Mead C and Conway L,** ***"Introduction to VLSI Systems",*** Addison Wesley, 1979.
6. **Glaser L and Dobberpuhl D,** ***"The Design and Analysis of VLSI Circuits",*** Addison Wesley, 1985.

**Course Outcomes**

**At the end of course, the students will be able to:**

CO1: Illustrate the overview of VLSI design methodology & layout design rules.

CO2: Understand the electrical properties and concepts of MOS inverter.

CO3: Design combinational logic circuits using CMOS logic.

CO4: Design sequential logic circuits like RAM design and CAM design.

CO5: Design any subsystem using digital logic.

## VLSI Design Practicals - I

**Semester I** **Hours of Instruction / week: 3P**
**19MEVC03** **No. of Credits: 1.5**

**Objective:**

To Simulate and implement digital Circuits using VHDL and Verilog HDL

**List of Experiments:**

1. Design of combinational and sequential circuits using VHDL
2. Design of combinational and sequential circuits using Verilog
3. Writing Test benches in VHDL / Verilog
4. Design Implementation using FPGA boards

**Tool Used: Xilinx ISE**

**Total Hours:45**

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Design and implement combinational and sequential circuits using VHDL and Verilog Hardware Description Language.

CO2: Simulate and analyze the propagation delay in digital circuits using test bench.

CO3: Implement digital circuits using FPGA boards.

## Microcontrollers and Programmable Digital Signal Processors Practicals

**Semester I** **Hours of Instruction / week: 3P**
**19MEVC04** **No. of Credits: 1.5**

**Objective:**

To implement the digital concepts using Microcontrollers and Programmable Digital Signal Processors.

**List of Experiments:**

**Part A)** Experiments to be carried out on Cortex-M3 development boards and using GNU toolchain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

**Part B)** Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points.
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

**Total Hours:45**

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.

CO2: Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

## Research Methodology and IPR

**Semester I** **Hours of Instruction/week: 4T**

**19MEVC05** **No. of Credits: 4**

**Objectives:**

To introduce the concept of Scientific Research and its processes and intellectual property rights.

**Unit I Introduction** **12**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

**Unit II Literature Survey** **12**

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

**Unit III Intellectual Property Rights** **12**

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

**Unit IV Patent Rights** **12**

Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

**Unit V New Development in IPR** **12**

Administration of Patent System, IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

**Total Hours: 60**

**Reference Books:**


1. ***Stuart Melville and Wayne Goddard,*** "***Research methodology: An introduction for science & engineering students*****",** Juta &Co Ltd, 1996.
2. ***Wayne Goddard and Stuart Melville***, "***Research Methodology: An Introduction*****",** Juta and company Ltd 2004.
3. ***Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners" 3rd Edition,*** *SAGE publications Ltd, 2014.*
4. ***Halbert,*** "***Resisting Intellectual Property***", Taylor & Francis Ltd, 2007.
5. ***Mayall, "Industrial Design",*** McGraw Hill, 2002.
6. ***Niebel,*** "***Product Design***", McGraw Hill, 2005.

7. ***Asimov*, "*Introduction to Design*",** Prentice Hall, 2000.
8. ***Robert P. Merges, Peter S. Menell, Mark A. Lemley**, "Intellectual Property in New Technological Age"*, 2016.
9. ***T. Ramappa*, "*Intellectual Property Rights Under WTO*"**, S. Chand, 2008

**Course Outcomes:**

**At the end of the course, the student will be able to:**

CO1: Outline the research problem.
CO2: Formulate the problem statement and prepare research plan for the problem under investigation
CO3: Discuss the Indian and International Intellectual Property Rights
CO4: Describe the patent rights
CO5: Discuss new developments in IPR

## Analog VLSI Circuits

**Semester II** **Hours of Instruction / week: 4T**
**19MEVC06** **No. of Credits: 4**

**Objective:**

To learn the basic building blocks of Analog circuit and also their design and verification.

**Unit I Analog Circuit Building Blocks 12**

Switches, active resistors - Current sources and sinks - Current mirrors/amplifiers Voltage and current references, Comparator (self-study).

**Unit II Amplifiers 12**

MOS and BJT inverting amplifier - Improving performance of inverting amplifier - CMOS and BJT differential amplifiers(self-study) - Characterization of Op-Amp - The BJT two stage op-amp - The CMOS two stage op-amp -Op-amps with output stage, Folded Cascode op-amp, Tran conductance Amplifier.

**Unit III Data Converter Fundamentals 12**

Ideal A/D and D/A converters, Quantization noise, Performance limitations. D/A And A/D Converters**:** D/A converter : Current scaling, Voltage scaling and Charge scaling D/A converters - Serial D/A converters - Serial A/D converters, Parallel - High performance A/D converters, Continuous time filters-Low pass filters - High pass filters(self-study) – Band Pass filters.

**Unit IV Design Automation and Verification 12**

Integrated circuit layout-Symbolic circuit representation (self-study)-Design rule Checks- Circuit Extraction – Digital circuit Simulation- Logic and Switch simulation- Timing analysis- Register Transfer- Level simulation.

**Unit V Analog Signal Processing Circuits & Analog Cell Layout, Layout Issues 12**

Modulators- Oscillators- Phase locked loops (self-study)-Layout Techniques- Resistor layout-Capacitor Layout- Analog cell layout. Mixed layout issues: Floor planning, power supply & ground, fully differential matching, Guard rings and shielding.

**Total Hours:60**

**References:**


1. **Randall L Geiger, Phillip E Allen and Noel R Strader,** ***"VLSI Design Techniques for Analog and Digital Circuits",*** McGraw Hill, International Edition, 1990.
2. **David A Johns and Ken Martin,** ***"Analog Integrated Circuit Design",*** John Wiley and Sons, 2002.
3. **Phillip Allen and Douglas Holberg,** ***"CMOS Analog Circuit Design",*** Oxford University Press, 2000.
4. **Jacob Baker R, Lee H W and Boyce D E,** ***"CMOS Circuit Design, Layout and Simulation",*** Prentice Hall of India, 1998.
5. **Paul R Gray and Robert G Meyer** ***"Analysis and Design of Analog Integrated Circuits",*** John Wiley and Son,2001.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Explain about the most important building blocks of analog ICs.

CO2: Analyze the importance and concepts of two stage CMOS op-amp, Folded Cascode op-Amp, Transconductance Amplifier.

CO3: Discuss the data converter fundamentals and its performance limitations.

CO4: Describe design automation and verification techniques of VLSI circuits.

CO5: Understand analog signal processing circuits and its layout issues.

## Testing and Testability

**Semester II** **Hours of Instruction / week: 4T**

**19MEVC07** **No. of Credits: 4**

**Objective:**

To understand testing of VLSI circuits using different testing techniques.

**Unit I Introduction 12**

Motivation for testing and design for testability(self study) - Fault models Combinational Circuit Testing**:** Test generation algorithms for combinational logic circuits - Fault Table, Boolean difference, Path sensitization, D - algorithm PODEM,FAN algorithms.

**Unit II Sequential Circuit Testing 12**

Functional testing –Fault model based testing- Time frame expansion.

**Unit III Fault Simulation Techniques 12**

Serial, Single-fault propagation, Deductive(self study), Parallel and Concurrent Simulation.

**Unit IV Design for Testability 12**

Key testability concepts – Ad Hoc design for Testability – scan based design - Signature analysis - Compression techniques(self study) -Built-in self-test Architectures.

**Unit V Special Testing Problems 12**

Memory testing techniques- Micro processor and Microcontrollers testing – Register decoding - Instruction decoding - data storage, transfer, manipulation functions - Testing analog components. Testability features for board test. FPGA testing (self study).

**Total Hours: 60**

**References:**


1. **Vishwani D Agarwal,** ***"Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits",*** Springer, 2000.
2. **Abramovici M, Breuer M A and Friedman A D,** ***"Digital Systems Testing and Testable Design",*** Wiley, 1994.
3. **Robert J Feugate and Jr Steven M,** ***"Introduction to VLSI testing",*** Prentice Hall, Englewood Cliffs, 1998.
4. **Parag K Lala,** ***"Digital Circuit Testing and Testability",*** **Academic Press, 1999.**


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Identify the significance of testable design.

CO2: Explain combinational and sequential circuit test generation algorithms.

CO3: Apply fault simulation techniques on digital circuits.

CO4: Use feasibility concepts.

CO5: Discuss testing of special circuits.

## VLSI Design Practicals – II

**Semester II** **Hours of Instruction / week: 3P**
**19MEVC08** **No. of Credits: 1.5**

**Objective:**

To understand the design and simulation of analog circuits using front end EDA tools

**List of Experiments:**

1. Design and Simulation of analog circuits using front end EDA tool
2. Design and Simulation of digital circuits using front end EDA tool
3. Timing and power analysis for analog circuit design using front end EDA tool
4. Generation of synthesis report using front end EDA tool

**Tools Used: Mentor Graphics Front end**

**Total Hours: 45**

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Design and Simulate analog and digital circuits using front end EDA tool.
CO2: Analyze the timing and power factor of analog circuit design.
CO3: Generate synthesis report for analog circuits.

## VLSI Design Verification and Testing Practicals

**Semester II** **Hours of Instruction / week: 3P**
**19MEVC09** **No. of Credits: 1.5**

**Objective:**

To verify and test VLSI system using EDA tools.

**List of Experiments:**

Verification and testing of

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

**Total Hours: 45**

**Course Outcomes**
**At the end of the course, the student will be able to:**
CO1: Verify increasingly complex designs more efficiently and effectively.
CO2: Use EDA tools like Cadence, Mentor Graphics.

**Program Elective - I**

**Computer Aided Design of VLSI Systems**

**Semester I** **Hours of Instruction / week: 4T**
**19MEVE11** **No. of Credits: 4**

**Objective:**

To study the design of VLSI circuits using CAD tools.

**Unit I Introduction 12**

VLSI Design cycle(self study) - Role of CAD tools in the VLSI Design process- Data Structures And Algorithms**:** Data Structures - Graph Theory – paths, trees, search algorithms, Complexity of algorithms, dynamic programming, Integer linear programming, Genetic algorithm, Simulated Annealing.

**Unit II Simulation & Synthesis 12**

Compiler driven simulation-Event driven simulation - Switch level simulation – Circuit simulation - logic synthesis – two level synthesis (self study), Binary decision diagrams, ROBDD principles.

**Unit III Physical Design Automation 12**

Partitioning - KL, FM algorithms, Placement – Simulation based algorithms- Simulated Annealing , Force Directed Algorithm, Partitioning based algorithms- Breuer's Algorithm, Terminal propagation Algorithm(self study) , Cluster Growth Algorithm , Floor planning – slicing floor plan ,Constraint Based Floor Planning, Integer Program Based Floor Planning – Pin Assignment.

**Unit IV Routing 12**

Grid routing – Maze Routing Algorithms, Global routing - Shortest Path Based Algorithms, Steiner tree based Algorithms, detailed routing – Left Edge algorithm, Dog-Leg Algorithm , Greedy Channel Routing(self study), Switch Box Routing algorithms- over the cell routing, Clock Routing.

**Unit V Layout Synthesis and Optimization 12**

Layout generation and Optimization of standard cell layout, gate matrix layout and PLA (self study), Layout Compaction – one dimensional and two dimensional compaction.

**Total Hours:60**

**References:**


1. **Sherwani N A,** ***"Algorithms for VLSI Physical Design Automation",*** Kluwer, 1999.
2. **Sait S M and Youssef H,** ***"VLSI Physical Design Automation",*** World Scientific, 1999.
3. **Sabih H Gerez,** ***"Algorithms for VLSI Design Automation",*** John Wiley & Sons, 1999.
4. **Micheli G D,** ***"Synthesis and Optimization of Digital Circuits",*** Tata McGraw Hill, 2004.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understanding of fundamental concepts in CAD and use VLSI design automation tools.
CO2: Perform simulation and high level synthesis.
CO3: Discuss floor planning and routing concepts.
CO4: Apply algorithms for placement and partitioning.
CO5: Describe layout compaction methods.

## Hardware Description Languages

**Semester I** **Hours of Instruction / week: 4T**
**19MEVE12** **No. of Credits: 4**

**Objective:**

To Learn the Architecture, Modeling, Tasks and functions of VHDL, Verilog with Examples

**Unit I Basic Concepts of Hardware Description Language 12**

Comparison between HDL and High Level Language Hierarchy, Concurrency, Logic and Delay Modeling, Structural, Data flow, Behavioural Styles (self study) of Hardware Description.

**Unit II VHDL 12**

Entity, architecture bodies, Identifiers, Data objects, Data Types, Operators, behavioral modeling data flow modeling, structural modeling, generics, configurations subprograms and overloading, packages and libraries, test benches (Self study).

**Unit III VERILOG 12**

Hierarchical Modeling concepts, Lexical conventions, Data types, System tasks, Compiler Directives, Modules and ports, Gate level modeling, Data flow modeling, Behavioural modeling.

**Unit IV Tasks and Functions 12**

Tasks and functions, Timing and Delays-Delay models, path delay modeling, Timing checks, Switch level modeling - Modeling elements, UDP - Combinational and Sequential UDPs (Self study), test benches (Self study).

**Unit V Hardware modeling examples 12**

Modeling delays, synchronous logic, state machine, Moore FSM, Mealy FSM, Clock divider, multiplier, barrel shifter, Digital filter (self study).

**Total Hours:60**

**References:**


1. **Bhasker J, *"A VHDL Primer",*** Prentice Hall, 1999.
2. **Bhaskar J, *"VHDL Synthesis Primer",*** Prentice Hall, 2nd Edition 1998.
3. **Bhasker J, *"A Verilog Primer",*** Prentice Hall, 1999.
4. **Bhaskar J, *"Verilog Synthesis Primer",*** Prentice Hall,1999.
5. **Stefan Sjoholm and Lennart Lindh, *"VHDL for Designers"*** 1997.
6. **Michael D Ciletti, *"Advanced Digital Design with Verilog HDL",*** Pearson education, 2005.
7. **Douglass Perry, *"VHDL",*** Tata McGraw Hill, McGraw-Hill Professional, 4th Edition, May 2002.
8. **Volnei A Pedroni, *"Circuit Design with VHDL",*** Prentice Hall, 2004.
9. **Samir Palnitkar, *"Verilog HDL: A Guide to Digital Design and Synthesis",*** Prentice Hall NJ, USA, 2003.
10. **Neil Weste and Kamran Eshranghian *"Principles of CMOS VLSI Design",*** Addison Wesley, 2000.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Analyze and design small scale combinational logic circuits using HDLs.

CO2: Analyze the problems in digital design using HDLs.

CO3: Effectively use a modern hardware description language (verilog) and computer aided design tools to implement designs in programmable devices.

CO4: Describe VLSI design from a hierarchical viewpoint.

CO5: Code state machines in a hardware description language.

## VLSI Signal Processing

**Semester I** **Hours of Instruction / week: 4T**
**19MEVE13** **No. of Credits: 4**

**Objective:**

To learn the various structures of Digital Signal Processing and their applications in VLSI Design.

**Unit I Introduction to Digital Signal Processing 12**

Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block diagram-SFG- DFG.

**UnitII Iteration bound, Pipelining and Parallel Processing of FIR Filter 12**

Data-Flow Graph Representations- Loop Bound and Iteration Bound-Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters- Parallel Processing- Pipelining and Parallel Processing for Low Power. Retiming: Definitions- Properties and problems- Solving Systems of Inequalities.

**Unit III Fast Convolution and Arithmetic Strength Reduction in Filters 12**

Cook-Toom Algorithm- Modified Cook-Toom Algorithm. Design of Fast Convolution Algorithm by Inspection. Parallel FIR filters-Fast FIR algorithms-Two parallel and three parallel. Parallel architectures for Rank Order filters-Odd Even Merge sort architecture-Rank Order filter architecture-Parallel Rank Order filters-Running Order Merge Order Sorter- Low power Rank Order filter.

**Unit IV Pipelined and Parallel Recursive Filters 12**

Pipeline Interleaving in Digital Filters- Pipelining in 1st Order IIR Digital Filters-Pipelining in Higher- Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.

**Unit V Scaling and Round off Noise 12**

Introduction to Scaling and Round off Noise- State Variable Description of Digital Filters- Scaling and Round off Noise Computation-Round Off Noise Computation Using State Variable Description- Slow-Down- Retiming and Pipelining.

**Total Hours: 60**

**Reference Books:**


1. **K.K Parhi:** ***"VLSI Digital Signal processing",*** John-wiley, 2nd Edition Reprint, 2008.
2. **John G.Proakis, Dimitris G.Manolakis, *"Digital Signal Processing",*** Prentice Hall of India, 1st Edition, 2009.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Explain the fundamentals of DSP.

CO2: Discuss pipelining and parallel processing of FIR filters.

CO3: Describe fast convolution and arithmetic reduction in filters.

CO4: Discuss pipelining and parallel processing of IIR filters.

CO5: Compute scaling and round off noise.

## Program Elective - II

## Microcontrollers and Programmable Digital Signal Processors

**Semester I** **Hours of Instruction / week: 4T**
**19MEVE21** **No. of Credits: 4**

**Objective:**

To learn the architecture of microcontrollers and programmable digital signal processors.

**Unit I ARM Cortex-M3 processor 12**

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers, Pipeline, Bus Interfaces.

**Unit II Exception and Interrupt 12**

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

**Unit III LPC Microcontroller 12**

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

**Unit IV Programmable DSP 12**

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC Unit, Barrel shifters, Introduction to TI DSP processor family.

**Unit V TMS320C6000 series Processor 12**

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processes, on chip peripherals, Processor benchmarking.

**Total Hours: 60**

**References:**


1. **Joseph Yiu, "The definitive guide to ARM Cortex-M3",** Elsevier, 2nd Edition.
2. **Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" ,** TMH , 2nd Edition.
3. **Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing",** Morgan Kaufman Publication.
4. **Steve furber, "ARM System-on-Chip Architecture",** Pearson Education.
5. **Frank Vahid and Tony Givargis, "Embedded System Design",** Wiley.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand the architecture and operations of ARM processor.

CO2: Discuss exception and interrupts of ARM processor.

CO3: Explore the functional blocks of LPC 17xx microcontroller.

CO4: Identify and characterize architecture of Programmable DSP Processors.

CO3: Develop small applications by utilizing the ARM processor core and DSP processor based platform.

## Digital System Design

**Semester I** **Hours of Instruction / week: 4T**

**19MEVE22** **No. of Credits: 4**

**Objective:**

To learn the basics of combinational circuits and sequential circuits and to design those using CPLDs and FPGAs.

**Unit I Introduction 12**

Boolean laws and theorems(self study) – use of Boolean algebra for simplification of logical expressions – Minterm and Maxterm – Canonical sum of products and product of sums expressions – Minimization of logical expressions using Karnaugh map.

**COMBINATIONAL CIRCUITS:** Combinational circuits and their design - Shannon's expansion theorem - Design using multiplexers and decoders.

**Unit II Synchronous Sequential Circuits 12**

Mealy machine - Moore machine - Design of synchronous sequential circuits - State diagram- State table- State reduction procedures by partitioning and implication chart- Minimal flip- flop/one-hot realization –Analysis of synchronous sequential circuits (self study).

**Unit III Asynchronous Sequential Circuits 12**

Design of asynchronous sequential circuits - Reduction of state and flow tables – Race – free state assignment –Incompletely specified sequential machines - Design of static hazard free and dynamic hazard free logic circuits - Essential hazards(self study) - Design of state machine using Algorithmic State Machines (ASM) chart as a design tool.

**Unit IV Programmable Logic Devices 12**

Basic concepts - Programming technologies - Programmable Logic Element (PLE) - Programmable Logic Array (PLA) and Programmable Array Logic (PAL) (self study) - Structure of Standard PLD's - Complex PLD's (CPLD) - System Design Using PLD's - Design of combinational and sequential circuits using PLD's- Introduction to Altera 7000 series CPLD.

**Unit V FPGAs 12**

Introduction to Field Programmable Gate Arrays - Types of FPGA - Xilinx XC3000 series - Logic Cell array(LCA) - Configurable Logic Blocks (CLB) - Input/Output Block (IOB) - Programmable Interconnect Point (PIP) - Introduction to Actel ACT1 family and Xilinx XC4000 family(self study).

**Total Hours: 60**

**References:**


1. **Charles H Roth**, " ***Digital System Design with VHDL***", Thomson, 1998.
2. **James E Palmer and David E Perlman**, "***Introduction to Digital Systems*** ", Tata McGraw Hill, 1996.
3. **Robert Dueck**, "***Digital Design with CPLD Applications and VHDL***", Thomson, 2004.
4. **Bob Zeidman**, "***Designing with CPLDs and FPGAs***", CMP, 2002.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Discuss the fundamentals of combinational circuits and sequential circuits.
CO2: Understand the concept of state machines.
CO3: Discuss about asynchronous sequential circuits and hazard free circuits.
CO4: Understand the concepts of programmable logic devices and CPLDs.
CO5: Explain about FPGAs.

## Neural Networks for VLSI

**Semester I** **Hours of Instruction / week: 4T**
**19MEVE23** **No. of Credits: 4**

**Objective:**

To introduce concepts of neural networks and their application in VLSI.

**Unit I Introduction and Basic Concepts 12**

Introduction- Humans and Computers, the structure of the brain, learning in machines, the differences. The basic neuron- Introduction, modeling the single neuron, learning in simple neurons, the perception: a vectorial perspective, the perception learning rule, proof, limitations of perceptrons.

**Unit II Multilayer Networks 12**

The multi layer perceptron: Introduction, altering the perception model, the new model, the new learning rule, multi layer perception algorithm, XOR problem. Multi layer feed forward networks, error back propagation training algorithm: problems with back propagation, Boltzman training, Cauchy training, combined back propagation, Cauchy training.

**Unit III Neural VLSI 12**

Hopfield memories – the first generation of neural network VLSI, Pattern classification using neural networks, Computational requirement, MOSFET equations – a crash course, Digital accelerators, Op-amps and resistors, Super threshold circuits for neural networks, Analogue/Digital combinations, MOS transconductance multiplier, MOSFET analogue multiplier, Imprecise low-area multiplier, Analogue , programmable – Intel Electronically Trainable Artificial Neural Network (ETANN) chip, Analogue synaptic weight storage – Dynamic weight storage, Metal Nitride Oxide Silicon(MNOS ) networks, Floating-gate technology, Amorphous silicon synapses.

**Unit IV Pulse Stream Technique 12**

Pulse encoding of information, Pulse stream arithmetic – addition and multiplication, Pulse stream communication, Pulse stream case studies – Edinburg SADMANN/ EPSILON work, The EPSILON chip, Process invariant summation and multiplication – the synapse, Pulse frequency modulation neuron, Pulse width modulation neuron, Switched-capacitor design, Per-pulse computation, EPSILON – The chosen neuron/synapse cells and results.

**Unit V Applications of Neural VLSI 12**

Real time speech recognition, Applications of neural VLSI – dedicated systems, Hardware co-processors, Embedded neural systems, The future - Hardware learning with multi-layer perceptrons, The top-down approach: Virtual Targets, The bottom-up approach : weight perturbation, Test problem, Weight perturbation for hardware learning, Noisy synaptic arithmetic – an analysis, Noise in training , On-chip learning.

**Total Hours:60**

**References:**


1. **R Beale & T Jackson,** ***"Neural Computing, An Introduction",*** Adam Hilger, 1990.
2. **Freeman J.A. and Skapura B.M,** ***"Neural Networks, Algorithms Applications and Programming Techniques",*** Addison Wesely, 1991.
3. **Alan Murray & Lionel Tarassenko ,** ***"Analogue Neural VLSI",*** Chapman & Hall, 1994.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Explain the concepts of neural networks.

CO2: Discuss the architecture, learning and application of multilayer neural networks.

CO3: Have knowledge of neural VLSI.

CO4: Understand Pulse Stream techniques in VLSI

CO5: Illustrate applications of neural VLSI.

**Program Elective - III**

**Image Security**

**Semester II** **Hours of Instruction / week: 4T**

**19MEVE31** **No. of Credits: 4**

**Objective:**

To learn the concepts of image Processing and to Learn the concepts in image security.

**Unit I Fundamentals of Digital Image Processing 12**

A simple Image Formation Model, Image Sampling, Equalization, Basic Gray level transformations – Arithmetic and Logic operations, Spatial Filters for Smoothening and Sharpening , Frequency Domain Filters for Smoothening , Sharpening.

**Unit II Color Image Processing 12**

Color Fundamentals, Color Models, Pseudo color Image Processing, Full Color Image Processing, Color Transforms, Smoothening and Sharpening of Color Images.

**Unit III Introduction to Image Security 12**

Cryptography – Algorithm – Concepts and Application – Steganography - Concepts of information hiding and Applications – Finger Printing - Concepts and Application.

**Unit IV Digital Watermarking 12**

Introduction to Digital Watermarking in copy right protection-Block diagram of watermarking system, importance of digital watermarking, applications of watermarking, Properties of watermarking system, imperceptibility, data pay load and robustness, evaluating watermarking system, Metrics, benchmarking, blind and non-blind algorithms, Comparing watermarking with communication.

**Unit V Attacks and Detection 12**

Embedding in DCT, DWT and DFT Domains, statistical detection, attacks on watermarked images, ensuring robustness.

**Total Hours: 60**

**References:**


1. **Rafael C. Gonzalez, Richard E.Woods,** "Digital Image Processing", 3rd Edition Pearson education, 2009.
2. **Cox, Miller and Talker, Bloom & Fridrich** "Digital Water Marking & Steganography", Morgan Kauffman Publiahers, 2008.
3. **Gonzalez, woods & Eddirs,** " DIP using Matlab" 2nd edition, Tata McGraw hill,2010.
4. **Neil F.Johnson,Zoran Duric, Sushel Jajodia "**Information Hiding - stegano-graphy & watermarking- attacks and counter measures", kluwer Academic publishers,2003.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand image enhancement techniques and apply them to gray scale images.
CO2: Perform the color image processing
CO3: Apply the Cryptographic and steganographic techniques for image security.
CO4: Explain the concepts of Digital watermarking for copy right protection.
CO5: Discuss embedding, extraction and issues of attacks on watermarked images

## Design Concepts in VLSI

**Semester II** **Hours of Instruction / week: 4T**

**19MEVE32** **No. of Credits: 4**

**Objective:**

To make students understand the design concepts in VLSI.

**Unit I INTRODUCTION** **12**

Overview of ASIC & FPGA Design flow, Advantages & limitations of FPGA design flow, Advantage and limitations of ASIC Design flow.

**Unit II DIGITAL DESIGN FLOW** **12**

HDL for verification and logic synthesis, Synthesis & simulation mismatches, Guidelines for modeling combinational logic circuits, Guidelines for modeling sequential logic circuits, Design for Verification, Design for Synthesis.

**Unit III BASICS OF FUNCTIONAL VERIFICATION** **12**

Need for functional Verification, Basic Terminologies – DUT, Test Bench, Response checker, Functional Verification for simple combinational( Multiplexer, Encoder, Decoder, Barrel Shifter) & Sequential Logic circuits( D flip flop, Synchronous & Asynchronous Counter, Shift register) Verification strategies – Black box, gray box and white box verification, Verification Tools – Simulators : Cycle based simulators, Event based simulators, Linting tools- Need for Linting process and limitation of Linting tools, Linting a HDL code, Waver form viewers, Coverage, Revision Control, Version Management, Introduction to Verification Methodologies

**Unit IV CONCEPTS OF LOGIC SYNTHESIS** **12**

Need for Logic synthesis, inputs and outputs in logic synthesis process, Logic synthesis – ASIC and FPGA perspective, Constraints management in logic synthesis process, synthesis constraints – overview of .sdc file format, Synthesis of Simple combinational logic circuits, Synthesis of Simple sequential logic circuits, Synthesis analysis - .sdf file format, reading the synthesis reports and design analysis, Synthesis optimization strategies – Need and focus areas

**Unit V TIMING ANALYSIS** **12**

Importance of Timing Analysis, Basics of Timing Analysis, Dynamic Timing Analysis – work flow, Concepts of Gate Level Simulation (GLS), Limitations of Dynamic Timing Analysis, Static Timing Analysis – Introduction, Basic Terminologies, inputs and outputs associated with Static Timing Analysis, Fundamentals of Static Timing Analysis, Analysis of Timing reports, Timing Optimization and design for performance

**Total Hours: 60**

**References:**


1. **M.J.S .Smith,** ***"Application Specific Integrated Circuits*****",** Addison -Wesley
   a. Longman Inc., 1997.
2. **Janick Bergeron "*Writing Test Benches – Functional Verification of HDL Models",*** Kluwer Academic Publishers
3. **J. Bhaskar "*Verilog HDL Synthesis*",** BS Publications, 2001.
4. **Andreas Meyer, "*Principles of Functional Verification*",** Newnes, 2003.
5. **Samir Palnitkar, "*Design Verification with e*",** Prentice Hall, 2003.
6. ***"IEEE Standard Verilog Language Reference Manual",*** IEEE Std 1364™-2001
7. ***"Prime Time User guide: Fundamentals",*** Version 2005.5

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand the concepts of ASIC Design flow and FPGA design flow.
CO2: Explain the concept of design for synthesis and design for verification.
CO3: Explain functional verification in digital design flow.
CO4: Discuss the logic synthesis.
CO5: Perform timing analysis for simple digital circuits.

## Mixed Signal VLSI Design

**Semester II** **Hours of Instruction / week: 4T**

**19MEVE33** **No. of Credits: 4**

**Objective:**

To make the students understand the design concepts using analog and digital signals.

**Unit I Introduction to Active Filters & Switched Capacitor Filters 12**

Active RC Filters for monolithic filer design: First & Second order filter realizations - universal active filter (KHN) - self tuned filter - programmable filters - Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits(self study) – Integrator- Biquad.

**Unit II Continuous Time Filters & Digital Filters 12**

Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors - BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance - Digital Filters: Sampling – decimation – interpolation (self study) - implementation of FIR and IIR filters.

**Unit III Digital to Analog & Analog To Digital Converters 12**

Non-idealities in the DAC - Types of DAC's: Current switched, Resistive(self study), Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's.

**Unit IV Sigma Delta Converters 12**

Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters(self study) - second order modulator - sigma delta DAC & ADC's.

**Unit V Analog and Mixed Signal Extensions to VHDL 12**

Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples. Analog Extensions to Verilog**:** Introduction - data types (self study)Expressions – Signals- Analog behavior –Hierarchical Structures –Mixed signal Interaction.

**Total Hours:60**

**References:**


1. **David A Johns and Ken Martin, *"Analog Integrated Circuit Design",*** John Wiley and Sons, 2002.
2. **Rudy van de Plassche *"Integrated Analog-to-Digital and Digital-to-Analog Converters",*** Kluwer, 1999.
3. **Antoniou, *"Digital Filters Analysis and Design",*** Tata McGraw Hill, 1998.
4. **Phillip Allen and Douglas Holberg *"CMOS Analog Circuit Design",*** Oxford University Press, 2000.
5. **Benhard Razavi, *"Data Converters",*** Kluwer Publishers, 1999.
6. **JacobBake R, Harry W Li, and David E Boyce *"CMOS, Circuit Design Layout and Simulation",*** Wiley- IEEE Press, 1st Edition Aug, 1997.
7. **Tsividis Y P, *"Mixed Analog and Digital VLSI Devices and Technology",*** Mc-Graw Hill, 1996.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Demonstrate in-depth knowledge in filter circuits.

CO2: Analyze the characteristics of different mixed- signal circuits.

CO3: Solve the engineering problems to increase the data rate of ADC and DAC.

CO4: Apply appropriate techniques to engineering activities in development of data converters.

CO5: Describe and simulate the analysis of mixed signals.

**Program Elective - IV**

**Low Power VLSI Design**

**Semester II** **Hours of Instruction / week: 4T**

**19MEVE41** **No. of Credits: 4**

**Objective**:

To make the students understand the need, analysis and estimation of low power devices and also study the different techniques to obtain low power.

**Unit I Introduction 12**

Introduction to low power VLSI design-Need for low power- Basic principles of low power design -Sources of Power dissipation (self study).

**Unit II Power Analysis and Estimation 12**

Power Analysis-Gate level analysis-Architecture level analysis-Probabilistic Power Analysis- Power estimation-Circuit level(self study)–-High level power estimation.

**Unit III Power Optimization Techniques 12**

Circuit -Logic - Special Techniques (self study) - Architecture and Systems.

**Unit IV Advanced Power Optimization Techniques 12**

Advanced Techniques - Low Power CMOS VLSI Design - Physics of Power Dissipation in CMOS FET Devices (self study).

**Unit V Low Power Static Ram Architectures 12**

Organization-MOS static RAM memory cell-banked organization (self study) -voltage swing reduction-power reduction

**Total Hours: 60**

**References:**


1. **Gary Yeap,** ***"Practical Low Power Digital VLSI Design",*** 2009.
2. **Kaushik Roy,** ***Sharat Prasad, "Low Power CMOS VLSI Circuit Design",*** 2009.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand the essential for low power design.

CO2: Study power analysis techniques.

CO3: Understand power optimization techniques in VLSI design.

CO4: Analyze architectures of RAM for low power design.

CO5: Study low power CMOS VLSI design.

## ASIC Design

**Semester II** **Hours of Instruction / week: 4T**
**19MEVE42** **No. of Credits: 4**

**Objective:**

To make the students understand the concepts of ASIC.

**Unit I Introduction to ASICS, CMOS Logic and ASIC Library Design 12**

Types of ASICs - Design flow (self study)- CMOS transistors CMOS Design rules - Combinational Logic Cell –Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance-Logical effort –Library cell design - Library architecture.

**Unit II Programmable ASICS, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells 12**

Anti fuse - static RAM - EPROM and EEPROM technology (self study)- PREP benchmarks - Actel ACT – Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

**Unit III Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry 12**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000(self study) - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language – PLA tools -EDIF- CFI design representation.

**Unit IV Logic Synthesis, Simulation and Testing 12**

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test – fault simulation (self study) - automatic test pattern generation.

**Unit V ASIC Construction, Floor Planning, Placement and Routing 12**

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow(self study) –global routing - detailed routing - special routing - circuit extraction - DRC.

**Total Hours:60**

**References:**


1. **M.J.S .Smith,** ***"Application Specific Integrated Circuits",*** Addison -Wesley Longman Inc., 1997.
2. **Farzad Nekoogar and Faranak Nekoogar,** ***From ASICs to SOCs: A Practical Approach,*** Prentice Hall PTR, 2003.
3. **Wayne Wolf,** ***"FPGA-Based System Design",*** Prentice Hall PTR, 2004
4. **R. Rajsuman, "*****System-on-a-Chip Design and Test".*** Santa Clara, CA: Artech House Publishers, 2000.
5. ***F. Nekoogar. "Timing Verification of Application-Specific Integrated Circuits (ASICs)". Prentice Hall PTR, 1999.***
6. **J.Bhaskar**, ***" A VHDL Synthesis Primer"*** BS Publications , 2001.
7. **J.Bhaskar,** ***"A Verilog HDL Primer"*** BS Publications, 2001.
8. **J.Bhaskar,** ***"Verilog HDL Synthesis"*** BS Publications, 2001.
9. **J.Bhaskar,** ***"VHDL Coding Styles and Methodologies"*** BS Publications, 2005.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Familiar with the concepts of ASIC.

CO2: Discuss about the memory concepts of ASIC.

CO3: Explain about the ASIC design software.

CO4: Describe about the testing methods.

CO5: Elaborate the construction and routing of ASIC.

## High Speed VLSI

**Semester II** **Hours of Instruction / week: 4T**
**19MEVE43** **No. of Credits: 4**

**Objective**:

Aims to provide high speed design techniques for use in VLSI design.

**Unit I Clocked Logic Styles 12**

Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.

**Unit II Circuit Design Margining and Design Variability 12**

Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

**Unit III Latching Strategies 12**

Latching Strategies, Basic Latch Design, Latching Differential Logic, Race Free Latches for Pre-charged Logic, Asynchronous Latch Techniques.

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**Unit IV Interface Techniques 12**

Signalling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design

**Unit V Clocking Styles 12**

Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

**Total Hours: 60**

**References:**


1. **Kerry Bernstein, Keith M. Carrig*, "High Speed CMOS Design Styles",*** Kluwer Academic Publishers, 2002.
2. **Evan Sutherland, Bob Stroll, David Harris," *Logical Efforts,Designing Fast CMOS Circuits",*** Kluwer Academic Publishers, 1999.
3. **David Harris*, "Skew Tolerant Domino Design",*** IEEE Journal of Solid State Circuits, 2001.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Describe circuits and techniques involved in high speed VLSI circuits.
CO2: Explore various design strategies to be followed for designing a high speed VLSI circuits.
CO3: Understand the latching styles for designing a high speed VLSI circuit.
CO4: Explain the interface techniques.
CO5: Discuss about the clocking styles.

**Program Elective - V**

**VLSI Design Signal Processing systems**

**Semester III** **Hours of Instruction / week: 4T**
**19MEVE51** **No. of Credits: 4**

**Objective:**

To learn the concepts of Signal processing in VLSI design systems.

**Unit I Unfolding 12**

Algorithm for Unfolding- Properties of Unfolding- Critical Path- Unfolding and Retiming- Applications of Unfolding. Folding: Folding Transformation- Register Minimization Techniques- Lifetime analysis-Data Allocation using forward-Backward register Allocation- Register Minimization in Folded Architectures- Folding of Multirate Systems.

**Unit II Digital Multiplier Architectures 12**

Parallel Multipliers- Interleaved Floor-plan and Bit-Plane-Based Digital Filters- Bit-Serial Multipliers- Bit-serial Filter Design and Implementation- Canonic Signed Digit Arithmetic- Distributed Arithmetic.

**Unit III Redundant Arithmetic 12**

Redundant Number Representations- Carry-Free Radix-2 Addition and Subtraction- Hybrid Radix-4 Addition- Radix-2 Hybrid Redundant Multiplication Architectures- Data Format Conversion- Redundant to Non redundant Converter. Numerical Strength Reduction: Sub expression Elimination- Multiple Constant Multiplication- Sub expression sharing in Digital Filters- Additive and Multiplicative Number Splitting.

**Unit IV Synchronous and Asynchronous Pipelining 12**

Synchronous Pipelining and Clocking Styles- Clock Skew and Clock Distribution in Bit- Level Pipelined VLSI Designs- Wave Pipelining- Constraint Space Diagram and Degree of Wave Pipelining- Implementation of Wave-Pipelined Systems- Asynchronous Pipelining- Signal Transition Graphs- Use of STG to Design Interconnection Circuits- - Implementation of Computational Units.

**Unit V Low Power VLSI DSP Systems 12**

Theoretical Background- Scaling Versus Power Consumption- Power Analysis- Power Reduction Techniques- Power Estimation Approaches.- Simulation Based Approach.

**Total Hours: 60**

**References:**


1. **K.K Parhi, *"VLSI Digital Signal processing",*** John-Wiley, 2008.
2. **Behrooz Parhami, *"Computer Arithmetic : Algorithms & HardwareDesigns",*** Oxford University Press, 2nd Edition, 2010.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Discuss the concepts of folding and unfolding in DSP systems.

CO2: Understand implementation of multipliers.

CO3: Explain in detail about redundant arithmetic concepts.

CO4: Elaborate on synchronous and asynchronous pipelining.

CO5: Gain knowledge on low power DSP systems.

**Genetic Algorithms and their Applications in VLSI**

**Semester III** **Hours of Instruction / week: 4T**

**19MEVE52** **No. of Credits: 4**

**Objective:**

To make students understand and apply the Genetic Algorithm as an optimization application for VLSI design.

**Unit I Fundamentals of Genetic Algorithm 12**

Terminologies – Simple Genetic algorithms – steady state algorithm – Genetic operators- types of GA-Genetic algorithms vs. Conventional algorithms – GA example – GA for VLSI design, layout and test automation.

**Unit II Partitioning 12**

Problem description – Circuit partitioning by genetic algorithms – hybrid genetic algorithms for ratio-cut partitioning.

**Unit III Placement and Routing 12**

Placement: Standard cell placement – Macro cell placement – Standard cell placement on a network of workstations. Routing: Steiner problem in graph – macro cell global routing

**UnitIV Genetic Algorithms in VLSI Testing 12**

Problem description – test generation frame work – test generation for test applications time reduction – deterministic/genetic test generators sequences dynamic test sequence compaction – parallel algorithms for ATPG.

**Unit V FPGA Technology Mapping and Peak Power Estimation 12**

FPGA technology mapping: Circuit segmentation and FPGA mapping-circuit segmentation for Pseudo-Exhaustive testing. Peak power estimation: Problem description – application of GA – Estimation of peak single cycle and n-cycle powers-peak sustainable power estimation.

**Total Hours: 60**

**References:**


1. **Pinaki mazumder and Elizabeth M Rudnick,"*Genetic algorithms for VLSI design layout and test automation*",** Pearson Edition, 2011.
2. **David E Goldberg, "*Genetic algorithms in search, optimization and machine learning*",** Addison-Wesley, Longman Publishing Co., Inc. Boston, MA, USA, 2009.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Discuss concepts on genetic algorithms.

CO2: Learn implementation of partitioning in genetic algorithms.

CO3: Understand implementation of genetic algorithms for placement and routing of VLSI circuits.

CO4: Use genetic algorithm for VLSI testing.

CO5: Familiarize with the use of genetic algorithm in FPGA technology mapping and peak power estimation.

## Computational Aspects of VLSI

**Semester III** **Hours of Instruction / week: 4T**

**19MEVE53** **No. of Credits: 4**

**Objective:**

To make the student understand the algorithms used for the VLSI design tools.

**Unit I Analysis and Design of Algorithms 12**

Abstract Data Types - Time and Space Analysis of Algorithms - Big Oh and Theta Notations Average, best and worst case analysis - Simple recurrence relations and use in algorithms – Mappings. **Algorithms Analysis** - Sorting - Searching - Design Techniques- Greedy Methods Dynamic Programming - Divide and Conquer - Back Tracking – Applications**.**

**Unit II VLSI Models 12**

Integrated circuits and the mead Conway rules-VLSI implementation of logic-Abstraction of VLSI circuits. **Lower bounds on area and time:** Introduction to lower bound arguments- information and crossing sequence probabilistic circuits and algorithms – circuits with repetitive inputs.

**Unit III Algorithm for VLSI Design 12**

Algorithms for layout –organization with high area- Compilation and optimization algorithms.

**Unit IV Overview of VLSI Design Systems 12**

Design languages- CIF –CHISEL –ESIM –LGEN- LAVA- SLIM- A regular expression language.

**Unit V Algorithms for VLSI Design Tools 12**

Reporting Intersections of Rectangles-Circuit Extraction Algorithms-Design Rule Checking- An Algorithm for Simulation of Switch Circuits-The PI Placement and Routing System- Optimal Routing.

**Total Hours: 60**

**References:**


1. **Jeffrey D. Ullman, "*Computational aspects of VLSI*",** Computer Science Press (1984).
2. **Alfred .V. Aho, John .E. Hop croft, Jeffrey .D. Ullman, "*Data Structures and Algorithms*",** Addison-Wesley Publications., 1985.


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand the concept of design and analysis of algorithms.

CO2: Learn the different models in VLSI.

CO3: Understand the compilation and optimization algorithms for VLSI Design.

CO4: Know about the design languages of VLSI Design system.

CO5: Understand the algorithms for VLSI Design tools.

**Open Elective**

**Waste to Energy**

**Semester: III** **Hours of Instruction / week: 4T**
**19MELO01** **No. of Credits: 4**

**Objective:**

To learn the energy obtained from waste and methods of conversion.

**Unit I Introduction 12**

Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

**Unit II Biomass Pyrolysis 12**

Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

**Unit III Biomass Gasification 12**

Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

**Unit IV Biomass Combustion 12**

Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

**Unit V Biogas 12**

Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

**Total: 60 Hours**

**Reference Books:**


1. **Ashok V., "Non Conventional Energy", Desai,** Wiley Eastern Ltd., 1990.
2. **Khandelwal, K. C. and Mahdi, S. S.**, "**Biogas Technology - A Practical Hand Book - Vol. I & II"**, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. **Challal, D. S., "Food, Feed and Fuel from Biomass",** IBH Publishing Co. Pvt. Ltd., 1991.
4. **C. Y. WereKo-Brobby and E. B. Hagan, "Biomass Conversion and Technology",** John Wiley & Sons, 1996.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand the various conversion devices used to obtain energy from waste.

CO2: Understand the methods used for yield and application of biomass pyrolysis.

CO3: Design and construct the gasifier engine for power generation.

CO4: Design and construct the biomass combustors.

CO5: Understand the types of biogas and various conversion methods.

**Audit Course-I**

**English for Research Paper Writing**

**(Non-credit Mandatory Course)**

**Semester I** **Hours of Instruction/week: 3T**
**19MEMA11**

**Objective:**

To make the students to write an effective research paper

**Unit I Planning and Preparation 9**

Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

**Unit II Findings and Review 9**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

**Unit III Review of the Literature 9**

Methods, Results, Discussion, Conclusions, the Final Check

**Unit IV Key skills 9**

Key skills are needed when writing a Title, key skills are needed when writing an abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

**Unit V Quality 9**

Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission and substantiated with valid research evidences

**Total Hours: 45**

**References:**


1. ***Goldbort R, "Writing for Science"***, Yale University Press (available on Google Books), 2006
2. ***Day R, "How to Write and Publish a Scientific Paper",*** Cambridge University Press, 2006
3. ***Highman N, "Handbook of Writing for the Mathematical Sciences",*** SIAM. Highman's book, 1998.
4. ***Adrian Wallwork, "English for Writing Research Papers",*** Springer New York Dordrecht Heidelberg London, 2011


**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand how to improve writing skills and level of readability

CO2: Learn about the writing method in each section

CO3: Understand and develop the research papers

CO4: Identify the key skills and useful phrases for writing good quality of paper

CO5: Substantiate with evidences for results and outcome.

**Disaster Management**
**(Non-credit Mandatory Course)**

**Semester I** **Hours of Instruction/week: 3T**
**19MEMA12**

**Objective:**

To provide board understanding about the basic concepts of disaster management

**Unit I Introduction** **9**

Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

**Unit II Repercussions of Disasters and Hazards** **9**

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

**Unit III Disaster Prone Areas in India** **9**

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

**Unit IV Disaster Preparedness and Management** **9**

Preparedness: Monitoring of Phenomena Triggering A Disaster Or Hazard; Evaluation of Risk: Application of Remote Sensing, Data From Meteorological and Other Agencies, Media Reports: Governmental and CommUnity Preparedness

**Unit V Risk Assessment and Disaster Mitigation** **9**

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co- Operation in Risk Assessment and Warning, People's Participation In Risk Assessment. Strategies for Survival. Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

**Total Hours: 45**

**References:**


1. ***R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies"*** New Royal book Company.
2. ***Sahni, PardeepEt.Al. (Eds.), "Disaster Mitigation Experiences and Reflections",*** Prentice Hall of India, NewDelhi.
3. ***Goel S. L., "Disaster Administration and Management Text and Case Studies"***, Deep & Deep Publication Pvt. Ltd., NewDelhi.

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Familiarize between natural and man-made disaster

CO2: Learn about the repercussions of disasters and hazards

CO3: Observe the various disaster prone areas in India

CO4:Describe the different monitoring phenomena, evaluation of risk and management

CO5: Understand the concepts of risk assessment and disaster mitigation

**Audit Course-II**

**Pedagogy Studies**

**(Non-credit Mandatory Course)**

**Semester II** **Hours of Instruction/week: 3T**
**19MEMA21**

**Objective:**

To provide the knowledge about pedagogy studies

**Unit I Introduction and Methodology 9**

Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education, Conceptual framework, Research questions**,** Overview of methodology and Searching.

**Unit II Thematic overview 9**

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

**Unit III Evidence on the effectiveness of pedagogical practices 9**

Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy. Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

**Unit IV Professional development 9**

Alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the commUnity, Curriculum and assessment, Barriers to learning: limited resources and large class sizes

**Unit V Research gaps and future directions 9**

Research design, context, Pedagogy, Teacher education, curriculum and assessment Dissemination and research impact

**Total Hours: 45**

**References:**


1. ***Ackers J. Hardman F, "Classroom interaction in Kenyan primary schools"***, Compare, 31 (2): 245-261. 2001
2. ***Agrawal M, "Curricular reform in schools: The importance of evaluation"***, Journal of Curriculum Studies, 36 (3):361-379. 2004
3. ***Akyeampong K, "Teacher training in Ghana - does it count?"*** Multi-site teacher education research project (MUSTER) country report 1. London: DFID. 2003
4. ***Akyeampong K, Lussier K, Pryor J, Westbrook J "Improving teaching and learning***

***of basic maths and reading in Africa: Does teacher preparation count?"*** International Journal Educational Development, 33 (3):272–282. 2013

5. ***Alexander RJ "Culture and pedagogy: International comparisons in primary education"***. Oxford and Boston: Blackwell. 2001
6. ***Chavan M, "Read India: Amassscale, rapid, 'learning to read' campaign"***. 2003

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand conceptual framework and terminology.

CO2: Develop Pedagogical practices used by teachers for the study.

CO3: Understand the effectiveness of pedagogical practices and methodology in depth.

CO4: Create professional development with classroom practices and know the barriers to learning.

CO5: Understand the research gaps and future directions of research impact.

**Value Education**

**(Non-credit Mandatory Course)**

**Semester II** **Hours of Instruction/week: 3T**
**19MEMA22**

**Objective**

Students will be able to understand value of education and self- development

**Unit I Values and self-development 9**

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

**Unit II Importance of cultivation of values 9**

Importance of cultivation of values - Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness, Honesty, Humanity, Power of faith, National Unity. Patriotism. Love for nature, Discipline

**Unit III Personality and Behaviour Development 9**

Personality and Behaviour Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness, Avoid fault Thinking,

**Unit IV Importance of Human Values 9**

Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature

**Unit V Importance of Character and Competence 9**

Character and Competence –Holy books vs Blind faith, Self-management and Good health. Science of reincarnation, Equality, Non-violence, Humility, Role of Women, All religions and same message, Mind your Mind, Self-control. Honesty, studying effectively

**Total Hours: 45**

**References:**

1. ***Chakroborty, S.K. "Values and Ethics for organizations Theory and practice",*** Oxford University Press, New Delhi

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: Understand the values of self-development.

CO2: Learn the importance of Human values.

CO3: Develop their personality.

CO4: Understand the importance of moral values in our life.

CO5: Cultivate Professional ethics.

**Community and Social Service (CSS)**

**(Non-credit Mandatory Course)**

**Semester II** **Hours of Instruction/Week: 2T**

**19MECS01**

**Objectives**

1. Create awareness on needs and problems of the community with special reference to women.
2. Understanding the programmes in operation for women's upliftment
3. Developing skills in organizing women into groups for collective action

**Unit I Profile of Women in India 6**

Profile of women in terms of literacy, work participation, health, reproductive health and nutrition and social and political participation. Survey to find out the literacy rate in different areas.

**Unit II Government Programmes for the upliftment of Women 6**

Education, Employment and Health

**Unit III Organizational support for Women 6**

Self help Groups, a strategy for Entrepreneurship among women. Role of NGOs for upliftment of women, organizing women into groups.

**Unit IV Women and Political Participation 6**

Need for political empowerment of women, 73$^{rd}$ amendment, 1/3$^{rd}$ reservation of women in Panchayat and local bodies performances, problems and prospects of elected women. Study the participation of women in local bodies

**Unit V Students involvement in community Social Services 6**

Data base on women – literacy, employment, issues related to work participation, marital problems and disability. Awareness generation programmes – child labour, violence against women, blood donation and legal provisions safeguarding women. Activities oriented: adult literacy and subject related activities

**Total hours: 30**

**References:**

1. ***Department of Home Science Extension, 2006, approaches to women and Development, Avinashilingam Institute for Home Science and Higher Education for Women, Coimbatore.***

**Course Outcomes**

**At the end of the course, the student will be able to:**

CO1: To possess the attributes of being morally and intellectually responsive with social awareness and a caring attitude for needy people.

CO2: To serve the community by applying their professional knowledge and skills.

CO3: To develop a right attitude of life, good interpersonal and communication skills, and a sense of social awareness.

CO4: To organize various types of community service activities and awareness programmes.